Early Evaluation of the SX-ACE Processor

Ryusuke Egawa, Kazuhiko Komatsu,
Hiroyuki Takizawa, and Hiroaki Kobayashi
Cyberscience Center
Tohoku University
Sendai, 980-8578, Japan
Email: {egawa, komatsu, tacky, koba}@isc.tohoku.ac.jp

Shintaro Momose, Yoko Isobe,
and Akihiro Musa
NEC Corporation
Tokyo, 108-8001, Japan
Email: {s-momose@ak, y-isobe@pi,
a-musa@bq}.jp.nec.com

***Abstract*—Using practical scientific and engineering applications, this poster presents early performance evaluation of the SX-ACE vector processor, which is the latest vector processor developed by NEC in 2013. While inheriting the advantages of the vector architecture, the SX-ACE processor is designed so as to overcome the drawbacks of conventional vector processors by introducing several architectural features. To unveil the potential of the SX-ACE processor, this poster evaluates and discusses how the brand-new vector processor is beneficial to achieve a high sustained performance on practical science and engineering simulations. Evaluation results show that, for a wide range of practical simulations, SX-ACE potentially achieves a higher sustained performance than its predecessor SX-9 and existing scalar processors.**

I. Introduction

To satisfy ever-increasing demands of computational scientists for a higher computational capability, the peak performance of a supercomputing system has drastically been improved. However, mainly due to the memory wall problem and several overheads to handle massive parallelism of the supercomputers, recent supercomputers have been involved in a deeper divergence between their theoretical and sustained performances. To overcome this situation, inheriting the advantages of conventional vector processors, the SX-ACE processor has been launched to provide a high memory bandwidth commensurate with its high computational capability. The SX-ACE processor is designed so as to meet the following two requirements for a higher sustained performance under the limited power and silicon budgets. One requirement is to achieve a high sustained memory bandwidth for accelerating memory-intensive applications. The other is to achieve a high single core performance for obtaining a practical level of sustained performance without excessively increasing the number of cores involved in parallel processing, because the parallel efficiency becomes lower if more cores are required to achieve a certain sustained performance.

In addition, the SX-ACE processor introduces several architectural features to overcome the drawbacks of its predecessor, SX-9. Assignable Data Buffer (ADB) and Miss Status Handling Register (MSHR) are implemented to make full use of the memory bandwidth by avoiding redundant memory transactions for vector load operations. Furthermore, the SX-ACE processor enhances the performances of short vector processing and indirect memory accesses by shortening memory access latency, introducing an out-of-order memory access mechanism, and a direct data-forwarding mechanism in pipeline chaining. As a result, the SX-ACE processor is expected to accelerate practical applications in various research fields.

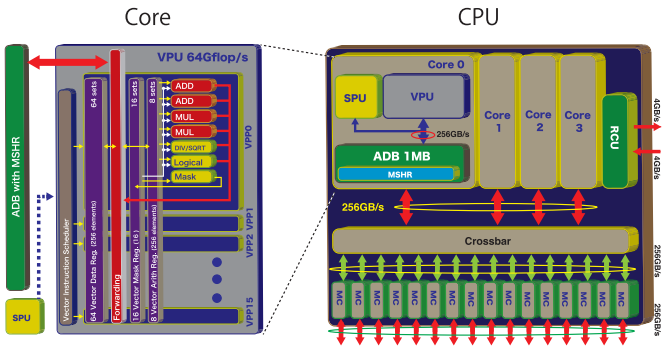

Fig. 1. SX-ACE Processor.

While the fundamental performance of the SX-ACE processor using common benchmarks is reported in [1], its potential for practical applications has not been analyzed well. Aiming to examine the potential of the SX-ACE processor, this poster evaluates the sustained performance of the SX-ACE processor, and analyzes how the architectural features can contribute to performance of practical scientific applications.

II. An Overview of The SX-ACE Processor

Figure 1 depicts an overview of the SX-ACE processor. The processor is composed of four cores, a memory control unit (MCU), a remote access control unit (RCU), and a memory crossbar. Each core consists of four major parts: a vector processing unit (VPU), a scalar processing unit (SPU), ADB, and MSHR. The aggregated performance of four cores reaches 256 Gflop/s with a 256 GB/s memory bandwidth provided by MCU.

Each core is connected to MCUs at a bandwidth of 256 GB/s through the memory crossbar, and four cores of one processor share the memory bandwidth of 256 GB/s through the memory crossbar. Due to this configuration, one core can exclusively utilize the entire memory bandwidth of 256 GB/s if the other three cores do not access the memory. Accordingly, the B/F ratio of each core can change from 1.0 up to 4.0 at maximum. VPU, which includes 16 vector pipelines and vector registers with a data-forwarding mechanism, is a key component of the SX-ACE processor with its single core performance of 64 Gflop/s. As well as previous SX series, the

TABLE I. EVALUATION ENVIRONMENTS.

Processor	Gflop/s/CPUs (Gflop/s/core, #. Cores)	Mem. GB/s	On-Chip Mem.	System B/F
SX-ACE	256 (64, 4 cores)	256	1MB ADB/core	1.0
SX-9	102.4 (102.4, 1 core)	256	256KB ADB/core	2.5
LX 406 (Ivy Bridge)	230.4 (19.2, 12 cores)	59.7	256KB L2/core 30MB shared L3	0.26
SR16000M1 (Power7)	245.1 (30.6, 8 cores)	128	256KB L2/core 32MB shared L3	0.52

TABLE II. EVALUATED APPLICATIONS.

Applications	Method	Memory access	Mesh Size	Code B/F	Actual B/F
QSFDM GLOBE	Spherical 2.5D FDM	Sequential	4.3×10^7	2.16	0.78
Barotropic	Shallow water model	Sequential	4322×2160	1.97	1.11
MHD (FDM)	FDM	Sequential	$2000 \times 1920 \times 32$	3.04	1.41
Seism3D	FDM	Sequential	$1024 \times 512 \times 512$	2.15	1.68
MHD (Spectral)	Pseudospectral Method	Stride	$900 \times 768 \times 96$	2.21	2.18
TURBINE	DNS	Indirect	$91 \times 91 \times 91 \times 13$	1.78	5.47
BCM	Navier Stokes Equation	Indirect	$128 \times 128 \times 128 \times 64$	7.01	5.86

SX-ACE processor can process up to 256 vector elements, 8 Bytes each, by a single vector instruction. The implementation of such an ample datapath is quite beneficial to high sustained performances of memory-intensive, practical applications.

An MCU has 16 memory interfaces of DDR3 and is connected to the memory composed of 16 DDR3 DIMMs with a 64 GB capacity through these interfaces. The memory is accessible from each core with a 128-Byte granularity. In order to improve the sustained memory bandwidth for indirect memory accesses and the performance of operations on short vector, the memory access latency is halved in comparison with the SX-9 processor.

III. PERFORMANCE EVALUATION OF THE SX-ACE PROCESSOR USING PRACTICAL APPLICATIONS

The sustained performance of the SX-ACE processor is evaluated by using seven practical applications. For comparison, the performances of processors on various supercomputers, which are listed in Table I, are also evaluated. Table II shows the outline of seven practical applications. The code B/F ratios of the applications in the table are obtained from the object codes of SX-ACE. In addition, to analyze the effects of on-chip memories and block data transfers between CPU and the memory subsystem, the actual B/F ratio measured on SX-ACE is also listed in the table.

Figure 2 shows the single processor performance, and their efficiencies of different systems for practical applications. The horizontal axis indicates the applications used in the evaluation. The bars indicate the sustained performances and the dots show the efficiencies of one processor on each supercomputing system. First, from these results, it is clarified that the SX-ACE processor achieves the highest performance among all the evaluated processors. This is due to the high sustained memory bandwidth of SX-ACE compared with the scalar-based systems. Since the actual B/F ratios of the applications are high, the memory performance of each system greatly

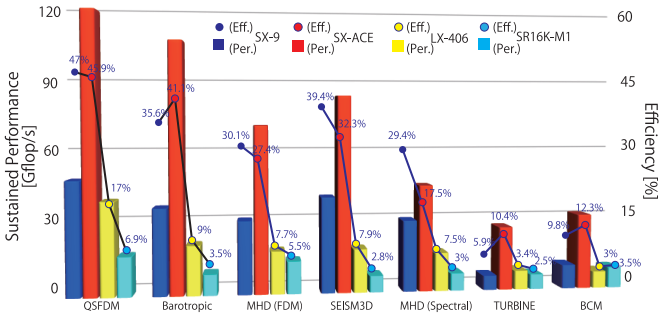

Fig. 2. Comparison in single CPU performance among multiple supercomputing systems.

affects the sustained performance of the applications. Thus, SX-ACE can achieve about 3.9× and 7.2× higher sustained performances than those of LX 406 and SR16000M1, respectively. On the other hand, compared with the SX-9 processor, SX-ACE achieves a higher sustained performance even though the memory bandwidth of the SX-9 processor is the same as that of the SX-ACE processor. This is because the new features of SX-ACE could successfully alleviate the high B/F ratio requirements in addition to the higher peak performance of the SX-ACE processor.

In terms of efficiencies, SX-ACE and SX-9 achieve higher efficiencies than the scalar processors. The high system B/F ratios of the vector processors bring the high efficiencies. Furthermore, the efficiencies of SX-ACE are comparable to those of SX-9 even though the system B/F ratio of SX-ACE is 40% lower than that of SX-9. Since the architectural features of SX-ACE contribute to the high sustained performance, the efficiencies of SX-ACE remain almost the same as those of SX-9. In particular, in the cases of Barotropic ocean, BCM, and TURBINE, the efficiencies are even higher than those of SX-9.

In the case of TURBINE, since its high cost kernels include short vector processing and indirect memory accesses, the performance of SX-9 is lower than those of scalar processors. However, the performance of SX-ACE is 2.3× and 3.3× higher than those of SR16000KM1 and LX 406, respectively. From these results, we can confirm that the architectural features of SX-ACE such as the large-capacity ADB with MSHR, the high-speed indirect memory accesses, and the enhanced short vector processing are not only overcoming the drawbacks of conventional vector processors, but also achieving a higher sustained performance compared with scalar processors.

IV. CONCLUSIONS

To clarify the potential of the SX-ACE processor, this poster examines its sustained performance using practical scientific applications. Evaluation results indicate that the SX-ACE processor has a higher potential to achieve a high sustained performance against the conventional vector and modern scalar processors. Our future work includes performance evaluation of the multi-node system, power evaluation, and performance comparison with GPUs/accelerators.

REFERENCES

[1] S. Momose, et.al, "The Brand-New Vector Supercomputer, SX-ACE," Proceedings of 29th International Supercomputing Conference (ISC'14), pp. 199 – 214, June 2014.